REMARKS

This amendment responds to the office action mailed November 19, 2003. In the office action the Examiner:

- allowed claims 1-7, 9, 10, 20, 31-34 and 50-73;
- rejected claims 11, 12, 15, 16, 18, 19, 21, 24-29, 35, 37, 40-45, 47 and 49; and
- objected to claims 13, 14, 17, 22, 23, 30, 36, 38, 39, 46 and 48.

Claims 1-7, 9, 10, 20, 31 and 50-73 are allowed. Claims 11-18, 21-28, 37-44 and 49 have been amended. Claims 74 and 75 have been added. After entry of this amendment, the pending claims are: claims 1-7 and 9-75.

In paragraph 3 of the Office Action, the Examiner rejected claims 11 and 12 under 35 U.S.C. § 102(e) as being anticipated by Woeste *et al.* Claims 11-14 have been amended.

Amended claim 11 now recites:

> 11. (Currently Amended) A method of operating a master/slave system, said method comprising the steps of:
>
> assessing a plurality of phase delays for synchronized communication between a master device and a slave device, wherein each phase delay is associated with a different bus connecting the master device and the slave device;
>
> .....

Woeste discloses an adaptive module for distributing clock signals to multiple slave modules with adaptive skew compensation. Col. 6, lines 40-50 and Figure 1A. For each slave module, the adaptive module includes a phase detector, control logic and a variable delay line. *Id.* The phase detector detects a phase difference between a reference clock signal and a feedback signal received from the slave module over a conductor. *Id.* The control logic device adjusts the delay factor of a variable delay line until the feedback signal is in phase with the reference clock signal. *Id.* The variable delay line then transmits a phase-adjusted variable clock signal to the slave module. *Id.*

Woeste fails to disclose or suggest "assessing a plurality of phase delays for synchronized communication between a master device and a slave device, wherein each

phase delay is associated with a different bus connecting the master device and the slave device," as claimed.

The failure of Woeste to show all of the elements of claim 11 vitiates any ground of rejection of claim 11 under 102(e). Applicant requests withdrawal of the rejection of claim 11 and allowance of claim 11, as amended.

Claim 12 depends from claim 11 and includes all the limitations of claim 11. Therefore, claim 12 is allowable for at least the same reasons as claim 11, and for the additional subject matter contained therein. Applicant requests withdrawal of the rejection of clam 12 and allowance of claim 12.

In paragraph 4, the Examiner rejected claims 15, 16, 18, 19, 21, 24-29, 35, 37, 40-45, 47 and 49 under 35 U.S.C. 103(a) as being unpatentable over Woeste in view of Ueda. Claims 15-18, 21-28, 37-44 and 49 have been amended.

Amended claim 15 now recites:

15. (Currently Amended) A master/slave system, comprising:

...

a master device coupled to the slave device and including an addressable phase value register bank adapted for storing a plurality of phase values for said slave device

....

As admitted by the Examiner, Woeste fails to disclose or suggest an addressable phase value register bank to store the phase values. The Examiner cites Ueda as curing the deficiencies of Woeste. Applicant disagrees.

Ueda generally discloses an intermittent receiving apparatus for use in a digital receiver for alternately carrying out receiving operations and non-receiving operations on a received carrier signal. Col. 1, lines 6-11. The apparatus includes a phase difference detection circuit 22, which is supplied with a reproduced clock signal and an oscillation signal from a clock reproduction circuit. Col. 4, lines 57-60. The phase difference detection circuit 22 detects a phase difference between the reproduced clock signal and the oscillation signal to produce a phase difference signal which is stored in a memory circuit 23. Col. 5, lines 3-9. At any given time, the memory circuit 23 stores only one phase difference signal, which is used to carrier out receiver operations and non-receiver operations on a received

carrier signal. Moreover, the phase difference signal has nothing to do with synchronized communication between a master device and a slave device.

Specifically, Woeste fails to disclose or suggest "a master device coupled to the slave device and including an addressable phase value register bank adapted for storing a plurality of phase values for said slave device," as claimed.

The failure of Woeste and Ueda, taken alone or in combination, to show or suggest all of the elements of claim 15 vitiates any ground of rejection of claim 15 under 103(a). Applicant requests the withdrawal of the rejection of claim 15 and allowance of claim 15, as amended.

Claims 16-19 depend from claim 15 and include all the limitations of claim 15. Therefore, claims 16-19 are allowable for at least the same reasons as claim 15, and for the additional subject matter contained therein.

Amended claim 21 now recites:

21. (Currently Amended) A method for calibrating transmission of data from a master device to a slave device over multiple buses, comprising:

determining phase offset values corresponding to the synchronous communication between the master device and the slave device over multiple buses;

storing the phase offset values in an addressable register bank in the master device to produce stored offset values; and

using the stored offset values in the synchronous communication between the master device and the slave device over at least one bus.

As previously explained above with respect to claim 15, Woeste fails to disclose or suggest an addressable phase value register bank to store the phase values, and the memory 23 disclosed by Ueda fails to cure this deficiency because it does not store more than one phase difference signal. Specifically, Ueda fails to disclose or suggest "determining phase offset values corresponding to the synchronous communication between the master device and the slave device over multiple buses," as claimed. Nor does Ueda disclose or suggest "storing the phase offset values in an addressable register bank in the master device to produce stored offset values," as claimed.

The failure of Woeste and Ueda, taken alone or in combination, to show or suggest all of the elements of claim 21 vitiates any ground of rejection of claim 21 under 103(a).

Applicant requests withdrawal of the rejection of claim 21 and allowance of claim 21, as amended.

Claims 22-30 depend from claim 21 and include all the limitations of claim 21. Therefore, claims 22-30 are allowable for at least the same reasons as claim 21, and for the additional subject matter contained therein.

Amended claim 37 now recites:

37. (Currently Amended) A method for calibrating transmission of information from a master device to a slave device, comprising:

...

determining a plurality of phase offset values for synchronizing communication between a master device and a slave device;

storing the phase offset values in an addressable phase value register bank in the master device to produce stored offset values;

....

Neither Woeste nor Ueda, taken alone or in combination, disclose or suggest "storing the phase offset values in an addressable phase value register bank in the master device to produce stored offset values," as claimed. Specifically, Woeste fails to show or suggest an addressable phase value register bank and the memory 23 disclosed by Ueda stores only one phase difference signal at a time.

The failure of Woeste and Ueda, taken alone or in combination, to show or suggest all of the elements of claim 37 vitiates any ground of rejection of claim 37 under 103(a). Applicants request withdrawal of the rejection of claim 37 and allowance of claim 37, as amended.

Claims 38-49 depend from claim 37 and include all the limitations of claim 37. Therefore, claims 38-49 are allowable for at least the same reasons as claim 37, and for the additional subject matter contained therein.

New claim 74 recites:

74. (New) A method of operating a master/slave system, said method comprising the steps of:

assessing a plurality of phase delays required for synchronized communication between a master device and a plurality of slave devices over a shared communication channel;

identifying a selected phase delay from said plurality of phase delays for a selected slave device of said plurality of slave devices; and

communicating information over said shared communication channel between said master device and said selected slave device of said plurality of slave devices in accordance with said selected phase delay.

New claim 75 recites:

75. (New) A master/slave system, comprising:

...

so as to establish synchronous communication between said master device and a selected slave device of said plurality of slave devices over a shared communication channel coupling said master device to each of said plurality of slave devices.

Neither Woeste nor Ueda, taken alone or in combination, disclose or suggest synchronized communication between a master device and a plurality of slave devices over a "shared communications channel," as claimed. For example, Woeste discloses a system where an adaptive module communicates with one or more slave modules over separate buses A, B C and D, and not a shared communications channel. See Figure 1A. Likewise, Ueda addresses an intermittent receiving apparatus for a digital receiver, and fails to disclose synchronous communication between a master device and slave device over a shared communication channel.

The failure of Woeste and Ueda, taken alone or in combination, to show or suggest all of the elements of claims 74 and 75 vitiates any ground of rejection of claims 74 and 75 under 102(e) and 103(a). Applicants request allowance of claims 74 and 75.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney if a telephone call could help resolve any remaining items.

Respectfully submitted,

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